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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/486,908	05/11/2000	STEFAN PFAB	P00.0365	9541

7590 02/08/2005

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EXAMINER	
ANDERSON, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/486,908	PFAB, STEFAN	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 15* is/are allowed.

6)☒ Claim(s) *1-7,9-14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Amendment

2. In response to the amendment filed 12/28/04:

claims 1, 8, 9, and 15 have been amended;

new claims 16-17 have been added.

Allowable Subject Matter

3. Claims 8 and 15 are allowed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 17 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be any support for the claim limitation regarding "said memory cells respond to a ***single*** data output request". In fact page 8, lines 12+ of the specification state that "in instance wherein the data representing a command proceed beyond the end of a memory cell field row (are contained in the next memory cell field row), two accesses on the data storage device must still be carried out in order to completely retrieve the appertaining command. The Examiner asks the Applicant to provide explicit citations from the disclosure to support this claim limitation.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-7, 9-14, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pawlowski (US Patent # 5,787,475).

8. With respect to claims 1 and 9, Pawlowski discloses a data storage device (main memory) (see column 4, lines 5-15) comprising:

memory cells having stored data with selectable output addresses (see column 4, lines 34-45, 54-60, and figure 1, item 14), wherein the specific starting address provided by a request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the requested data and outputs the requested data with cache lines, which are considered to be the selected output start address;

wherein the storage device (main memory) responds to a data output request (peripheral device) by outputting the stored data beginning with a selected output start address (see column 4, lines 34-45 and column 5, line 66 to column 6, lines 10; and column 6, lines 19-35 and 50-59), wherein the specific starting address provided by the request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the request data, and outputting the requested data with cache lines or consecutive cache lines, which are considered to be the selected output start address;

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data in response to the data output request (see column 6 lines 30-35; column 7, lines 15-25; column 9 line 56 to column 10, line 15; column 11, lines 45-58, and column 11, line 64 to column 12, line 8). Data retrieved by the I/O controller to determine which cache line of data contains the beginning portion of address requested by the peripheral from the memory. If this beginning portion of the address is in the first cache line, then the data output to requested data by the first cache line. However, if the retriever determines that a next consecutive cache line contains the beginning portion of the requested data, the retriever increments the starting address and uses the incremented starting address to request the consecutive cache lines of data from memory. In all situations, a first cache line of consecutive cache lines, the data stored in the neighboring starting address is less than the output address since if the portion of the starting address provided by the requested data is in the first cache line, the output transfers to requested data by first cache line; and if it is greater than the first cache line, the output transfers by two consecutive cache lines.

9. With respect to claims 2 and 10, Pawlowski discloses a the selected output start address (beginning portion of started address for outputting the data requested by a cache line) is determined utilizing address data (peripheral device) applied to the data storage device (main memory) (see column 4, lines 34-45 and column 5, line 66 to column 6, line 10).

10. With respect to claims 3 and 11, Pawlowski discloses:

the selected output start address is determined by further utilizing adaptation data (data retriever) applied to the data storage (main memory) (see column 9, lines 22-42; and column 9, line 64 to column 10 line 15);

the adaptation data (data retriever) is related both to the output start address to be employed and an address that is defined by the address data (peripheral device) (see column 6, lines 30-35).

11. With respect to claims 4 and 12, Pawlowski discloses:

output terminals (main memory output terminals) (see figure 1, items 14 and 26);

an interface (I/O module) provided between memory cell of the data storage device (main memory) and the output terminals (see figure 1, items 14, 18, 24, 26, and figure 2, items 16, 42, 44, and column 6, lines 19-25).

12. With respect to claim 6, Pawlowski discloses using a prefetch system wherein the first cache line and second cache connected as a consecutive cache line for transferring the data to a requested data (peripheral device), and based on the beginning portion of the address provided by the requested data, if the starting address is greater than the first cache line, a consecutive line will be retrieved (see column 4, lines 54-60; column 5, line 66 to column 6, line 19, and column

7, lines 15-25). In other words, data stored with an output start address selected from the group consisting of a first output start address and a second output start address are through-connected.

13. With respect to claims 7 and 14, Pawlowski discloses the first output start address (beginning portion of the address provided by peripheral device for cache line output from the main memory) is an address that is represented by the address data (peripheral device) applied to the data storage device (main memory) (see column 5, line 59 to column 6, line 10).

14. With respect to claims 5 and 13, Pawlowski discloses a multiplexer that is driven based on the adaptation data, by showing in figure 2, data buffered from the data retriever is input into an I/O interface 44.

15. With respect to claims 1 and 9, Pawlowski teaches all other limitations, as discussed above, but fails to specifically disclose a data storage device in a single integrated circuit unit. The Applicants' own specification though states in page 3, lines 11+, that "the data storage devices can also fundamentally be a matter of other, arbitrary data storage devices." Therefore, it would have been obvious to one skilled in the art to incorporate the memory module and I/O module of Pawlowski into a single integrated circuit in order to increase processing speeds. See also MPEP 2144.04 as to why integration, or the use of a one piece construction instead of the structure disclosed in the prior art would be merely a matter of obvious engineering choice, and would not be patentably distinct. (See also *In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)* and *In re Tomoyuki Kohno 391 F.2d 959; 55CCPA 998; 157 USPQ (BNA) 275.*)

16. With respect to claim 16, Pawlowski teaches all other limitations, as discussed above, but fails to specifically disclose wherein the device is selected form the group consisting of a RAM, a ROM, EPROM, and a flash EPROM. The Applicants' own specification though states in page 3, lines 11+, that "the data storage devices can also fundamentally be a matter of other, arbitrary data storage devices." Therefore, it would have been obvious to one skilled in the art to use one of the above memory types as the memory device of Pawlowski in order to provide the desired volatile or nonvolatile memory according to preferred engineering choices such as speed, reliability, etc..

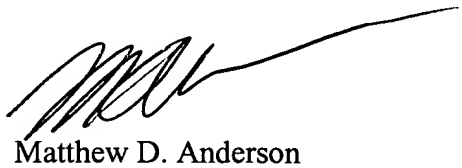
17. With respect to claim 17, Pawlowski teaches all other limitations, as discussed above, but fails to specifically disclose the memory cells responding to a single data output request. While Pawlowki may make a prefetch request for a second line of data, page 8, lines 12+ of the Applicants' specification state that "it should also be *obvious* that, in instance wherein the data representing a command proceed beyond the end of a memory cell field row (are contained in the next memory cell field row), two accesses on the data storage device must still be carried out in order to completely retrieve the appertaining command. Accordingly, it would have been obvious to one skilled in the art to use the memory request of Pawlowski in order to completely retrieve the desired data from memory if the proceeds beyond the end of a memory row.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (571) 272-4177. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Matthew D. Anderson
Primary Examiner
Art Unit 2186